C3 cont'd

way, the MCM 10 can provide a reduced interconnect lead and a low inductance chip to decoupling capacitor connection.--

Please replace the paragraph beginning at page 10, line 18, with the following rewritten paragraph:

--Figures 3A - 3B depict one particular embodiment of a decoupling capacitor 30 that can be employed with the MCM 10 depicted in Figure 1. The depicted decoupling capacitor 30 is a component that is mounted to the support base 12 before the interconnect layer 16 is formed. The decoupling capacitor 30 can comprise a thin film MCM-D technology fabricated device, and in particular can be formed by multi-layer thin film processing with copper or aluminum metallization and SiO_2 dielectric material fabricated on a silicon base as shown in Figure 2. One such capacitor and techniques for forming such a capacitor is generally described in the above referenced U.S. Patent 5,134,539.--

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In the claims:

Claims 12 and 21-33 are pending. Pursuant to 37 C.F.R. §1.121(c)(3), please replace pending claims 12 and 21 with replacement claims 12 and 21, as set forth below. A marked-up version of the claims follows the Remarks. Please cancel claim 23, without prejudice.

Replacement claim 12:

12. (Twice Amended) A device for interconnecting a plurality of circuit devices, comprising:

a decoupling capacitor mounted on a first surface; and

an interconnect layer having a pattern of circuit connections and being formed over said decoupling capacitor, whereby electrical connections of said decoupling capacitor are embedded within said interconnect layer and said interconnect layer is disposed between said decoupling capacitor and said plurality of circuit devices,

and whereby said pattern of circuit connections of said interconnect layer is coupled to said decoupling capacitor and said plurality of circuit devices.

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